CLAIMS

We claim:

1.   A method in a computer system of decompressing data that has been subject to compression and the compressed data being in a set of predetermined data layers, the computer system including a host processor connected via a peripheral bus to a secondary processor, the method comprising the steps of:

10   decompressing at least a system layer of the compressed data in the host processor; and
           decompressing other data layers of the set in the secondary processor.

2.   The method of Claim 1, wherein the secondary
15   processor is a graphics accelerator.

3.   The method of Claim 1, wherein the secondary processor is a dedicated MPEG decompression circuit for decompression of data subject to MPEG compression.
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4.   The method of Claim 1, wherein the step of decompressing at least a system layer further comprises decompressing a book layer of the set.

25   5.   The method of Claim 1, wherein the data includes audio and video data.

6.   The method of Claim 1, wherein the step of decompressing other data layers includes the steps of:
30   variable length decoding the compressed data;
           inverse zig-zagging the decoded data;
           inverse quantizing the zig-zagged data, and
      inverse discrete cosine transforming the inverse quantized data.
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7.   The method of Claim 1, wherein the step of decompressing other data layers includes motion vector compensation of the data.

8.   A computer system adapted for decompression of compressed data which is in a set of predetermined data layers, comprising:

        a host processor;
        a peripheral bus connected to the host processor;

        a secondary processor connected to the peripheral bus; and

        means for decompressing in the host processor at least a system layer of the compressed data, wherein other data layers of the set are decompressed in the secondary processor.

9.   The system of Claim 8, wherein the secondary processor is a graphics accelerator.

10.   The system of Claim 8, wherein the secondary processor is a dedicated decompression circuit for decompression of data which has been compressed using MPEG compression.

11.   The system of Claim 8, wherein the means for decompressing at least a system layer further comprises decompressing means for decompressing a book layer of the set.

12.   The system of Claim 8, wherein the data includes audio and video data.

13.   The system of Claim 8, wherein the means for decompressing at least the system layer includes:
        means for variable length decoding the

-32-

33

compressed data;

    means for inverse zig-zagging the decoded data; and

    means for inverse quantizing the data.

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    14. The system of Claim 8, wherein decompression of the other layers of the set includes motion vector compensation of the data.

10   15. The computer system of Claim 8, further comprising a frame buffer connected to the secondary processor.

    16. A frame reconstruction circuit for
15 reconstructing a block of video data that has been subject to MPEG compression, the block of video data including a plurality of pixels arranged in a horizontal and vertical array, and comprising:

    a first interpolation element having an input
20   terminal for receiving data representing the pixels of the block of video data, wherein the first interpolation element averages data representing a first pixel of the block of data with data representing a second pixel adjacent in
25   a first direction in the block of data to the first pixel, and providing the averaged value at an output terminal;

    a second interpolation element having an input terminal coupled to the output terminal of
30   the first interpolation element, wherein the second interpolation element averages an averaged value from the first interpolation element with an averaged value from the first interpolation element associated with a set of pixels of the
35   block of data adjacent in a second direction orthogonal to the first direction, the second

-33-

34

interpolation element having an output terminal for providing the average of the two averaged values at the output terminal; and

a selector element having an input terminal coupled to the output terminal of the second interpolation element, wherein the selector element selectably provides at its output terminal a value representing one of:

a)   an externally provided signal;

b)   the average of the two averaged values from the second interpolation element;

c)   a sum of the externally provided signal and the average of the two averaged values.

17.   The circuit of Claim 16, further comprising a first storage element coupled between the output terminal of the first interpolation element and the input terminal of the second interpolation element, and a second storage element coupled between the output terminal of the second interpolation element and the input terminal of the selector element.

18.   The circuit of Claim 16, wherein the first interpolation element includes:

a flip-flop having an input terminal and an output terminal, the flip-flop input terminal being coupled to the input terminal of the first interpolation element;

a multiplexer having a control terminal, first and second input terminals, and an output terminal, the input terminals of the multiplexer being coupled respectively to the input terminal of the first interpolation element and to the output terminal of the flip-flop; and

an adder having two input terminals coupled

respectively to the output terminal of the
multiplexer and the output terminal of the flip-
flop, and having an output terminal coupled to the
output terminal of the first interpolation

5 element.

19. The circuit of Claim 16, wherein the second
interpolation element includes:
        a shift register having an input terminal
10 coupled to the input terminal of the second
interpolation element and having an output
terminal;
        a multiplexer having two input terminals
coupled respectively to the output terminal of the
15 shift register and the input terminal of the
second interpolation element, a control terminal,
and an output terminal; and
        an adder having two input terminals coupled
respectively to the output terminal of the shift
20 register and to the output terminal of the
multiplexer, and having an output terminal coupled
to the output terminal of the second interpolation
element.

25   20. The circuit of Claim 19, wherein the shift
register includes:
        an n stage shift register element, where n $\geq$
8;
        a one-stage shift register element; and
30   a multiplexer having two input terminals
connected respectively to an output terminal of
the n stage shift register element and to an
output terminal of the one-stage shift register
element.
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        21. The circuit of Claim 16, wherein the selector

-35-

36

element includes:

a first multiplexer having two input
terminals connected respectively to the output
terminal of the second interpolation element and
5   to a reference value;, and having an output
terminal and a control terminal;

a second multiplexer having two input
terminals connected respectively to receive the
externally provided signal and a reference value,
10   and having an output terminal and a control
terminal; and

an adder having two input terminals coupled
respectively to the output terminals of the first
and second multiplexers, and having an output
15   terminal coupled to the output terminal of the
selector element.

22.   The circuit of Claim 16, wherein the input
terminal of the first interpolation element and the
20   output terminal of the selector element are each 8-bit
parallel data ports, and the circuit has at least an
internal bus structure of at least 8 bits.

23.   The circuit of Claim 16, further comprising a
25   second data path for bidirectional processing,
comprising:

an additional first interpolation element;
and

an additional second interpolation element;
30   wherein each of the additional interpolation
elements are serially coupled in parallel to the
first and second interpolation elements.

24.   The circuit of Claim 16, further comprising a
35   feedback path coupling the output terminal of the
selector element to the input terminal of the first

-36-

37

interpolation element.

25. The circuit of Claim 16, wherein one of the first and second interpolation elements is a horizontal interpolation element, another being a vertical interpolation element.

26. A method of reconstructing a block of video data that has been subject to MPEG compression, the block including a plurality of pixels arranged horizontally and vertically in an array, the method comprising:

first, selectively averaging values associated with two pixels adjacent in a first direction in the block;

second, selectively averaging two of the selectively averaged values associated with two sets of pixels adjacent in a second direction orthogonal in the first direction; and

selectively providing as an output signal one of:

a) an externally provided signal;

b) a result of the second step of selectively averaging; and

c) a sum of the externally provided signal and the result of the second step of selectively averaging.

38